Pole-Zero Analysis of Multi-Stage Amplifiers: A Tutorial Overview

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(Invited Paper)

Abstract—Analyzing pole-zero locations of an amplifier is essential to 1) understand the characteristics of a circuit in the frequency domain, and 2) choose appropriate frequency compensation techniques to guarantee the stability of a circuit over a specified range of load resistance and capacitance. The objective of this paper is to provide tutorial treatment of the steps for analyzing poles and zeros in multi-stage amplifiers. These techniques can be equally applied for the analysis of power management circuits such as low-dropout voltage regulators (LDOs) and controllers for DC-DC converters.

Index Terms—Frequency compensation, pole-zero analysis, two-stage amplifiers, multi-stage amplifiers, cascode compensation, current buffers, LHP zero.

I. INTRODUCTION

Finding the analytical equations of poles and zeros is often essential to 1) choose appropriate frequency compensation techniques to stabilize an amplifier and 2) understand which parameters have more impact than others, aiding in tuning the circuit for desired frequency response. In this tutorial, we explain the process of performing small-signal analysis and deriving the equations of poles and zeros in two-stage and three-stage amplifiers. Section II outlines the steps for finding poles and zeros. Section III illustrates pole/zero analysis in a two-stage folded-cascode op-amp. Section IV shows an example of analyzing poles and zeros for a more complex three-stage amplifier. SPICE simulations are performed to compare hand-computed pole/zero locations with AC analysis.

II. STEPS FOR FINDING POLES/ZEROS

The steps for obtaining the DC gain, poles and zeros of a circuit are

1) Draw the small-signal model
2) Apply Kirchhoff’s Current Law (KCL) at each node
3) Solve the KCL equations using symbolic manipulation software to obtain the transfer function
4) Set s=0 to find the DC gain of the amplifier
5) Factor and solve the numerator to obtain zeros
6) a) Applying the assumption of widely-separated poles, solve the denominator to obtain the poles, OR
       b) Applying the assumption of widely-separated poles with complex pole pair, solve the denominator to obtain the poles

III. POLE-ZERO ANALYSIS OF TWO-STAGE AMPLIFIER

Compensation networks such as Miller compensation [2]–[4], cascode compensation [1], [5]–[8], nested Miller compensation (NMC) [9], [10], and reverse NMC (RNMC) [6], [11] are widely used techniques to stabilize multi-stage amplifiers.

The transistor-level schematic of a two-stage op-amp using cascode compensation is shown in Fig. 1. This circuit is adapted from Fig. 3 of [1]. The first stage is a PMOS folded cascode differential amplifier and the second stage is a PMOS common-source amplifier. The transconductance, output resistance and lumped parasitic capacitance of the first and second stage are represented by \( g_{m1}, g_{m2}, R_1, R_{OUT}, C_1 \) and \( C_{OUT} \) respectively. The first stage is inverting so as to ensure that the overall gain from \( V_{IN+} \) to \( v_{OUT} \) is non-inverting. Equations for the small-signal parameters of the amplifier are given in Table I and the small-signal model is shown in Fig. 2. A system with three reactive elements \( (C_1, C_{OUT}, C_C) \) typically give rise to three poles.

IV. CONCLUSION

The first-stage differential amplifier is represented with voltage-controlled current source (VCCS) \( g_{M1}v_s \), where \( v_s \) is the differential input voltage, given by \( v_s \equiv V_{IN+} - V_{IN-} \). The output of the first-stage is \( v_1 \). The second-stage is represented with VCCS \( g_{M2}v_1 \). The output of the second-stage is \( v_{OUT} \). The compensation capacitor \( C_C \) and resistor \( R_C \) are connected between \( v_{OUT} \) and \( v_X \), where \( v_X \) is the source node of the common-gate transistor \( M_6 \). Transistor \( M_6 \) acts as a positive current buffer between \( v_X \) and \( v_1 \) represented...
with VCCS $g_{mB}V_X$. If $C_{gd9}$ is large (as in the case of a LDO pass transistor), it must be placed in Fig. 2 as a capacitor between nodes $v_1$ and $v_{OUT}$. Transistor $M_6$, resistor $R_C$ and compensation capacitance $C_C$ form the cascode compensation. The impedance looking into the source terminal of $M_6$ is $1/g_{mB}$, connected between nodes $v_X$ and ground. Resistor $R_C$ can be used to increase the impedance looking into the source to $1/g_{mB} + R_C$, as illustrated in [6], [7].

### TABLE I

<table>
<thead>
<tr>
<th>Small-signal Parameters of Two-Stage Amplifier (Fig. 2)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_{m1}$</td>
<td>$g_{m1}M_1M_2$</td>
</tr>
<tr>
<td>$R_1$</td>
<td>$r_{oi}</td>
</tr>
<tr>
<td>$C_1$</td>
<td>$C_{gd4}C_{gd6}+C_{gd9}$</td>
</tr>
<tr>
<td>$g_{m2}$</td>
<td>$g_{m9}$</td>
</tr>
<tr>
<td>$R_{OUT}$</td>
<td>$r_{oM}</td>
</tr>
<tr>
<td>$C_{OUT}$</td>
<td>$C_{gd9}+C_{gd10}+C_L$</td>
</tr>
<tr>
<td>$g_{mB}$</td>
<td>$g_{m9}M_6$</td>
</tr>
</tbody>
</table>

* Omitting bulk capacitance for simplicity

### A. Applying Kirchhoff’s current law (KCL)

In order to obtain the transfer function of the amplifier shown in (1), we apply KCL at every node in Fig. 2. Let $i_C$ be the current flowing through the compensation network from node $v_{OUT}$ to node $v_X$. The set of KCL equations are

$$g_{mB}v_X = g_{m1}v_S + \frac{1}{R_1} + v_1sC_1$$

$$i_C = \frac{(v_{OUT} - v_X)}{R_{OUT}(1/sC_C)} = \frac{v_X}{g_{mB}}$$

$$0 = i_C + g_{m2}v_1 + \frac{v_{OUT}}{R_{OUT}} + v_{OUT}C_{OUT}$$

### B. Transfer Function

Solve the equations in (2) so as to eliminate $v_1, v_x$ and $i_C$ to obtain the transfer function $G(s) = v_{OUT}(s)/v_S(s)$ in (1) using symbolic manipulation software. The transfer function of a two-stage amplifier with three left-half-plane (LHP) poles and one LHP zero has a general form given by

$$G(s) = A_{DC}\left(\frac{1+s\omega_{Z1}}{1+b_1s+b_2s^2+b_3s^3}\right)$$

1) **DC Gain:** $A_{DC}$ is the DC gain of the amplifier, given by the product of the gains of the two stages as

$$A_{DC} \equiv G(s)|_{s=0} = g_{m1}R_1g_{m2}R_{OUT}.$$

2) **Three Real Poles:** The general equation of a transfer function with three real LHP poles $\omega_{P1}, \omega_{P2}, \omega_{P3}$ and single LHP zero $\omega_{Z1}$ is

$$G(s) = \frac{A_{DC}\left(1+s\omega_{Z1}\right)}{(1+b_1s+b_2s^2+b_3s^3)}$$

The coefficients for $s, s^2$ and $s^3$ in the expanded denominator of the transfer function in (3) are compared with those of the transfer function in (3) as shown below:

$$b_1 = \frac{1}{\omega_{P1}} + \frac{1}{\omega_{P2}} + \frac{1}{\omega_{P3}}$$

$$b_2 = \frac{1}{\omega_{P1}^2\omega_{P2}} + \frac{1}{\omega_{P2}^2\omega_{P3}} + \frac{1}{\omega_{P3}^2\omega_{P1}}$$

$$b_3 = \frac{1}{\omega_{P1}^2\omega_{P2}^2\omega_{P3}}$$

Assuming widely separated poles ($\omega_{P1} \ll \omega_{P2} \ll \omega_{P3}$), the coefficients of $s, s^2$ and $s^3$ can be approximated as

$$b_1 \approx \frac{1}{\omega_{P1}} \Rightarrow \omega_{P1} \approx \frac{1}{b_1}$$

$$b_2 \approx \frac{1}{\omega_{P1}\omega_{P2}} \Rightarrow \omega_{P2} \approx \frac{1}{b_2}$$

$$b_3 \approx \frac{1}{\omega_{P1}\omega_{P2}^2} \Rightarrow \omega_{P2} \approx \omega_{P1}\omega_{P3}$$

### C. Calculating Pole Locations

The two-stage amplifier in Fig. 2 has three real poles if the output capacitor $C_{OUT}$ is very large; otherwise, it has a complex pole pair.

1) **Three Real Poles:** Assuming real and widely separated poles, the equation for the dominant pole $\omega_{P1}$ is given by

$$\omega_{P1} = \frac{1}{b_1} = -1/(R_{OUT}C_C + R_CC_C + R_{OUT}C_{OUT})$$

$$+ C_C/g_{mB} + R_C C + g_{m2}R_{OUT}$$

In order to simplify this expression, we make the following assumptions concerning small-signal parameters

$$R_1, R_{OUT} \gg R_C \quad \text{and} \quad g_{m1}R_1, g_{m2}R_{OUT} \gg 1$$

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$$+ C_C/g_{mB} + R_C C + g_{m2}R_{OUT}$$
Applying (12), that is, neglecting smaller terms,

$$\omega_{P1} \approx -1/R_1C_m g_m R_{OUT}.$$  \hfill (13)

Substituting the $\omega_{P1}$ in (7), the equation of first non-dominant pole $\omega_{P2}$ is given by

$$\omega_{P2} = \frac{\omega_{P1}}{b_2} = -\left( g_m R_{OUT} g_m R_1 C_C / (R_1 C_m g_m + R_{OUT} C_{OUT} g_m R_1 C_C + R_1 C_g R_{OUT} C_C + R_1 C_m R_1 C_m R_{OUT} C_C + R_1 C_g R_{OUT} C_C). \right.$$  \hfill (14)

Applying the assumptions in (12), $\omega_{P2}$ is approximated as

$$\omega_{P2} \approx \frac{1}{(1/g_m) C_1 \left( 1 + \frac{C_{OUT}}{C_C} \right)}. \hfill (15)$$

Observe the equations of the dominant pole $\omega_{P1}$ in (13) and first non-dominant pole $\omega_{P2}$ in (15). As the value of compensation capacitor $C_C$ increases, the dominant pole $\omega_{P1}$ moves to lower frequencies, whereas the non-dominant pole $\omega_{P2}$ moves to higher frequencies. The two poles moving apart as the compensation capacitor increases is known as pole splitting, and generally helps in improving the stability of the amplifier.

Substituting $\omega_{P1}$ and $\omega_{P2}$ in (7), the high frequency pole $\omega_{P3}$ is given by

$$\omega_{P3} = -\frac{C_C + C_{OUT}}{C_C C_{OUT} (R_C + 1/g_m B)} \hfill (16)$$

In a design example, when we input realistic values for small-signal parameters of Table I, we found that the calculated values for $\omega_{P2}$ and $\omega_{P3}$ were very close to each other, violating the assumption that the real poles are widely separated. Hence, we anticipate the existence of a complex pole pair.

2) One Real Pole and One Complex Pole Pair: For moderately-sized $C_{OUT}$, the two non-dominant poles converge and form a single complex pole pair. The dominant pole $\omega_{P1}$ is unchanged and is given by (13).

Applying the assumptions from (12), the non-dominant complex pole $\omega_{P2}$ and quality factor $Q$ are given by

$$\omega_{P2} \approx \sqrt{\frac{g_m B g_m C_1}{C_C C_{OUT}}} \hfill (17)$$

$$Q \approx \frac{C_C}{(C_C + C_{OUT}) \sqrt{g_m B C_1}} \hfill (18)$$

D. One Real Zero

The equation of the LHP zero is given by

$$\omega_{Z1} = -\frac{1}{C_C (R_C + 1/g_m B)}. \hfill (19)$$

Table II summarizes the derived equations of the poles and zeros. The third column in the table represents the hand-calculated values. Fig. 3 illustrates the pole/zero locations before and after compensation.

### Table II: Pole/Zero Equations of Fig. 1 and their Approximate Values

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Equation</th>
<th>Value/Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_{DC}$</td>
<td>$g_m R_1 g_m R_{OUT}$</td>
<td>50dB</td>
</tr>
<tr>
<td>$\omega_{P1}$</td>
<td>$\frac{1}{R_1 C_m g_m R_{OUT}}$</td>
<td>40kHz</td>
</tr>
<tr>
<td>$\omega_{P2}$</td>
<td>$\sqrt{\frac{g_m B g_m C_1}{C_C C_{OUT}}}$</td>
<td>28MHz</td>
</tr>
<tr>
<td>$Q$</td>
<td>$\frac{C_C}{(C_C + C_{OUT}) \sqrt{g_m B C_1}}$</td>
<td>0.78</td>
</tr>
<tr>
<td>$\omega_{Z1}$</td>
<td>$\frac{1}{C_C (R_C + 1/g_m B)}$</td>
<td>24MHz</td>
</tr>
<tr>
<td>$\omega_{GBW}$</td>
<td>$\frac{g_m}{C_C}$</td>
<td>14MHz</td>
</tr>
</tbody>
</table>

Fig. 3. Diagram illustrating pole/zero locations (not to scale).

E. Bandwidth and Phase Margin

The gain-bandwidth product is given by

$$\omega_{GBW} \approx A_{DC} \omega_{P1} = \frac{g_m}{C_C} \hfill (19)$$

The phase margin for a system with three real poles and single zero is computed using the equation given by

$$PM \approx 90^\circ - \tan^{-1} (\alpha_2) - \tan^{-1} (\alpha_3) + \tan^{-1} \left( \frac{\omega_{GBW}}{\omega_{Z1}} \right), \hfill (20)$$

where $\alpha_2 \equiv \omega_{GBW} / \omega_{P2}$ and $\alpha_3 \equiv \omega_{GBW} / \omega_{P3}$. If there exist a complex pole pair, the phase margin becomes

$$PM \approx 90^\circ - \tan^{-1} \left( \frac{\alpha_2}{Q (1 - \alpha_2)} \right) + \tan^{-1} \left( \frac{\omega_{GBW}}{\omega_{Z1}} \right). \hfill (21)$$

F. Comparison with SPICE Simulation

SPICE simulation for circuit shown in Fig. 1 is performed to compare the analytical pole/zero locations. Fig. 4 shows the AC analysis simulated result of two-stage amplifier shown in Fig. 1, when driving a nominal load of 10k$\Omega$|100pF. The hand-calculated DC gain and unity gain frequency given in Table II are very close to the simulated values. The calculated phase margin is 69.8$^\circ$ and the simulated phase margin is 60$^\circ$.

Fig. 4. Simulated loop gain and phase response of the two-stage amplifier driving 10k$\Omega$|100pF, with the theoretical pole and zero locations indicated.
IV. Pole-Zero Analysis of Three-Stage Amplifier

The three-stage pseudo class-AB amplifier shown in Fig. 5 is the NMOS version of the circuit in [12]. The first stage is a differential amplifier and the next two stages are common-source amplifiers. The PMOS transistor $M_{10}$, which is an inverting common-source amplifier, creates a feed-forward path $g_{mF}$ from the intermediate node to the output node. The last stage of the amplifier is a non-inverting common-source amplifier. It comprises an NMOS current mirror formed by $M_9$ and $M_{11}$ of dimensions in $1:K$ ratio, as shown in Fig. 5.

![Schematic of three-stage amplifier based on [12].](image)

RNMC with nulling-stage amplifier is adopted to stabilize the amplifier for a wide range of capacitive loads. The small-signal model of this three-stage amplifier is shown in Fig. 6.

![Small-signal model of three-stage amplifier shown in Fig. 5.](image)

Using notations similar to the previous example, $i_{C1}$ and $i_{C2}$ are the currents flowing through the compensation network from node $v_{OUT}$ to node $v_1$ and from node $v_2$ to node $v_1$, respectively. Apply KCL at every node in Fig. 6, to obtain the set of equations:

\[
\begin{align*}
  i_{C1} + i_{C2} &= g_{m3}v_3 + \frac{v_1}{R_1} + v_1sC_1 \\
  i_{C1} + i_{C2} &= \frac{v_2-v_3}{R_1C_1} \\
  i_{C1} &= \frac{v_{OUT}-v_2}{1/sC_2} \\
  i_{C2} &= \frac{v_2-v_3}{1/sC_2} \\
  0 &= i_{C2} + g_{m2}v_2 + \frac{v_3}{R_2C_2} + v_2sC_2 \\
  g_{m3}v_2 &= i_{C1} + g_{mF}v_1 + \frac{v_{OUT}}{R_{OUT}} + v_{OUT}sC_{OUT}
\end{align*}
\]

Solving these equations as illustrated in previous example, so as to eliminate $v_1$, $v_2$, $i_{C1}$ and $i_{C2}$ the DC gain, poles and zeros are derived as shown in Table III.

The amplifier has four poles. $C_{21}$ creates the dominant pole. The effect of the next two non-dominant poles can be nullified by proper placement of the two LHP zeros created by RNMC. The fourth pole is at very high frequencies. As a result, the overall amplifier response can be designed to behave as a two-pole system with widely-separated poles.

As a design example, the simulated frequency response of the three-stage amplifier driving a load of $10k\Omega||100pF$ is shown in Fig. 7.

![Simulated loop gain and phase response of the three-stage amplifier driving 10kΩ||100pF, with the theoretical pole and zero locations indicated.](image)

### References


