Converting a Three-Stage Pseudo-Class AB Amplifier to a True Class AB Amplifier
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Abstract—We convert a low-voltage, low transistor-count, wide swing multi-stage pseudo-class AB amplifier proposed in [1] to a true class AB amplifier. The conversion is made possible using gate-drain feedback to combine two inverting common-source amplifiers to form a single non-inverting stage. Both the pseudo-class AB and true class AB amplifiers were fabricated in a 0.5 μm CMOS 2P3M process. They are designed to operate from ±1.25 V supplies at a nominal quiescent current of 175 μA and a minimum phase margin of 45° when driving capacitive loads from 1 pF to 200 pF and resistive loads from 1 kΩ to 1 MΩ. The total compensation capacitance of the proposed class AB amplifier is 12 pF, 50% less than the pseudo-class AB amplifier. The simulated unity-gain frequency of the class AB amplifier is 4.9 MHz at a load of 25pF/|1kΩ|, 88% higher than that of the pseudo-class AB amplifier. Experimental measurements show that the proposed amplifier has a maximum total bias current of 175 μA, compared to 1.05 mA for the pseudo-class AB amplifier. Measured slew rates of the proposed amplifier are 2.7 V/μs and 3.3 V/μs, double those of its pseudo-class AB counterpart.

Index Terms—Class AB amplifier, pseudo-class AB amplifier, nested Miller compensation, reverse nested Miller compensation, gate-drain feedback.

I. INTRODUCTION

CLASS AB amplifiers have a wide range of applications in portable electronic devices, as they can generate output currents that are much greater than the total bias current in the output stage [2]. Class AB amplifiers are found in such circuits as audio amplifiers, motor drivers and LED and LCD drivers [3]. These applications generally require amplifiers with low quiescent power, high efficiency, rail-to-rail output swing, high slew rate and stability for a wide range of capacitive and resistive loads.

As technology advances, design parameters such as transistor length and supply voltage are decreasing. The consequence is a reduction in gain for a single-stage amplifier. The best method to achieve high gain is by cascading single-stage amplifiers, where the total gain is the product of the gains of each stage. On the other hand, the complexity of the compensation scheme increases with the number of cascaded stages [4], [5]. Widely-used compensation techniques for multi-stage amplifiers are nested Miller compensation (NMC) [6], [7] and reverse NMC (RNMC) [1], [7]–[10].

The pseudo-class AB amplifier in Fig. 1 is an NMOS version of the amplifier in [1]. It is a high-gain, multi-stage amplifier with a very simple biasing circuit, low transistor-count and wide output swing. The amplifier can operate with low supply voltages and currents. As such, the amplifier has been adopted in a wide range of applications [11]–[14].

The major disadvantage of the pseudo-class AB amplifier is power consumption. Because of the current mirror formed by transistors $M_9,M_{11}$ at the output stage, the total bias current of the amplifier increases proportionately with the output sinking current. In this paper, we propose a low-power three-stage class AB amplifier with transistor count, biasing circuit and maximum output currents that are similar to those of the pseudo-class AB amplifier. However, the proposed class AB amplifier has the advantage of low total bias current that does not increase with output current.

The design and analysis of the three-stage pseudo-class AB amplifier are described in Section II for the purpose of comparison with the proposed class AB amplifier, which is described in Section III. Section IV details hardware and simulation results. We conclude our work in Section V.

II. THREE-STAGE PSEUDO-CLASS AB AMPLIFIER

The schematic of the three-stage pseudo-class AB amplifier based on [1] is shown in Fig. 1. The first stage ($M_1$–$M_5$) is a differential amplifier. The next two stages are common-source amplifiers. The first common-source amplifier ($M_6$–$M_7$) has negative gain and the second one ($M_8$–$M_{11}$) has positive gain. The PMOS transistor $M_{10}$, which is an inverting common-source amplifier, creates a feed-forward path from the intermediate node to the final output to produce the push-pull action for the amplifier.

The last stage of the amplifier includes an NMOS current mirror formed by $M_9$–$M_{11}$ with a dimension ratio of $1:K$. Since $M_{11}$ is the output transistor, it can pass a large sinking current, resulting in a correspondingly large current through

![Fig. 1. Schematic of three-stage pseudo-class AB amplifier from [1].](image-url)
the mirror transistor $M_0$. Thus the total bias current is increased when the output is sinking current, resulting in the loss of efficiency; hence the designation pseudo-class AB amplifier.

The pseudo-class AB amplifier can be compensated with RNMC, cascode compensation [15]–[17], or split-length transistor compensation [4]. The major disadvantage of Miller compensation (with no nulling resistor) is that it introduces a right half-plane (RHP) zero. Cascode compensation and split-length transistor compensation, introduce left half-plane (LHP) zeros. However, cascode compensation has the drawback of increased static power consumption and transistor count, if applied to the amplifier shown in Fig. 1, since there are no cascode transistors. Moreover, both cascode compensation and split-length transistor compensation cannot move the LHP zero to a desired location easily. Adding a nulling resistor in series with the Miller capacitor not only moves the RHP zero to the LHP, but also offers freedom in selecting the approximate location of the zero [18]. Therefore, as shown in Fig. 1, we have adopted RNMC ($C_{C1}, C_{C2}$ and $R_C$) to stabilize the amplifier for a wide range of capacitive loads.

![Small-signal model of three-stage pseudo-class AB amplifier](image)

The small-signal model of the amplifier in Fig. 1 is given in Fig. 2. The transconductance of the first stage is $g_{m1}$ and subsequent stages are $g_{m2}$ and $g_{m3}$. The transconductance of the feed-forward path is $g_mF$. The impedances to ground at nodes $V_1$, $V_2$, and $V_{OUT}$ are $R_1||C_1, R_2||C_2$ and $R_{OUT}||C_{OUT}$, respectively. The gain of the amplifier is approximately the product of the gains of all three stages and is given by

$$A_V = g_{m1}R_1(g_{m2}R_2g_{m3}R_{OUT} + g_mF)$$

$$A_V \approx g_{m1}R_1g_{m2}R_2g_{m3}R_{OUT}$$

(1)

We conducted AC small-signal analysis for the pseudo-class AB amplifier in Fig. 1. Assuming $C_{C1}, C_{C2}, C_{OUT} \gg C_1, C_2$ and widely separated poles and zeros, the amplifier has four LHP poles and two LHP zeros. The equations of the poles and zeros with corresponding frequencies that were calculated using simulated DC operating point values are given in Table I. The compensation capacitance $C_{C1}$ creates the dominant pole. The effect of the next two non-dominant poles $\omega_{P2}$ and $\omega_{P3}$ can be mitigated by proper placement of the two LHP zeros $\omega_{Z1}$ and $\omega_{Z2}$ created by RNMC. The last pole $\omega_{P4}$ is a high frequency pole; its effect on stability is nearly negligible.

The first non-dominant pole $\omega_{P2}$ is highly dependent on $C_{OUT}$, whereas the zeros $\omega_{Z1}$ and $\omega_{Z2}$ are dependent on $C_{C1}$ and $C_{C2}$. When the value of $C_{OUT}$ is large, $\omega_{P2}$ moves to low frequencies and the value of the compensation capacitors $C_{C1}$ and $C_{C2}$ that would cancel $\omega_{P2}$ may become prohibitively large.

### III. Proposed Three-Stage Class AB Amplifier

The schematic of the proposed three-stage class AB amplifier is shown in Fig. 3. The first stage ($M_1$-$M_3$) is a differential amplifier. Three inverting common-source amplifiers follow the differential stage. The first two inverting common-source amplifiers ($M_6$-$M_7$ and $M_8$-$M_9$) are combined with gate-drain feedback to behave as a single non-inverting common-source stage. The output stage is formed by the inverting common-source amplifiers $M_{10}$-$M_{11}$. PMOS transistor $M_{10}$ provides the feed-forward path from node $V_1$ to the output node.

![Schematic of proposed three-stage class AB amplifier](image)

All internal stages have constant bias current, generated through NMOS current mirrors $M_{12}$-$M_5$,$M_7$-$M_9$, whereas the output stage has large sourcing and sinking capability. Bias currents through the output stage transistors $M_{10}$ and $M_{11}$ is $I_{b2}$ because $M_6$ and $M_{10}$ have identical gate-source voltage. The maximum sourcing current through $M_{10}$ is limited by the common-mode input voltage applied to $V_{IN+}$ and $V_{IN-}$. On the other hand, the maximum sinking current through $M_{11}$ is only limited by the supply voltage. This confirms the true class AB operation of the output stage.

The proposed class AB amplifier employs both NMC and RNMC techniques to achieve adequate phase margin. Compensation network $C_{C1}/R_{C1}$ with $C_{C2}/R_{C2}$ form NMC and $C_{C1}/R_{C1}$ with $C_{CS}/R_{CS}$ form RNMC.
A. Gate-drain Feedback

The overall gain and effective number of stages of the proposed class AB amplifier are decreased by introducing gate-drain feedback resistor $R_{GD}$ across the second common-source amplifier. The presence of $R_{GD}$ nullifies the gain of the first common-source amplifier and helps in moving the internal pole at node $V_{GD}$ to high frequencies. Since the gain of the second common-source amplifier is inverting, applying Miller's theorem [4], the resistance at the output node $V_2$ is approximately equal to the gate-drain feedback resistor

$$R_{GD,OUT} = R_{GD} \left(1 + \frac{1}{g_{mGD}R_{GD}} \right) \approx R_{GD}. \quad (2)$$

The gain of the second common-source amplifier is therefore

$$A_{VCS2} = -g_{mGD} (R_{GD,OUT}||r_{ao}||r_{ao}) \approx -g_{mGD}R_{GD} \quad (3)$$

where $r_{ao}$ is the drain resistance of transistor $M_i$. Applying Miller's theorem [4], the resistance at the input node $V_{GD}$ is reduced by the gain of the second common-source amplifier

$$R_{GD,IN} = \frac{R_{GD}}{1+g_{mGD}R_{GD}} \approx \frac{R_{GD}}{g_{mGD}} = \frac{1}{g_{mGD}} \quad (4)$$

Now the gain of first common-source amplifier is

$$A_{VCS1} = -g_{m2} (R_{GD,IN}||r_{ao}||r_{ao}) \approx -\frac{g_{m2}}{g_{mGD}}. \quad (5)$$

Therefore the gain of the second stage non-inverting common-source amplifier, which is the cascade of the first two inverting common-source amplifiers, is simply

$$A_V = A_{VCS1} \cdot A_{VCS2} = g_{m2}R_{GD}. \quad (6)$$

B. Small-Signal Model

The small-signal model of the proposed class AB amplifier is shown in Fig. 4. Small-signal parameters are the same as those defined earlier. The gain of the class AB amplifier is approximately the product of the gains of all three stages

$$A_{DC} \approx g_{m1}R_1g_{m2}R_{GD}g_{m3}R_{OUT}. \quad (7)$$

Assuming $C_{C1}, C_{C2}, C_{C3}, C_{OUT} \gg C_1, C_2$ and widely separated poles and zeros, the class AB amplifier has four LHP poles and three LHP zeros. The equations of all poles and zeros with calculated frequency values are summarized in Table II. The dominant pole is determined by the compensation capacitor $C_{C1}$, the first-stage output resistance $R_1$, and the gain of amplifier stages covered by $C_{C1}$. The next two non-dominant poles $\omega_{P2}$ and $\omega_{P3}$ can be cancelled by proper placement of the first two LHP zeros $\omega_{Z1}$ and $\omega_{Z2}$. Therefore, the amplifier is approximated as a two-pole/single-zero system. The effect of the last pole $\omega_{P4}$ can be nearly eliminated by adjusting the location of the third zero $\omega_{Z3}$. However, cancellation cannot be exact, since $\omega_{P4}$ is a function of load capacitance $C_{OUT}$.

![Fig. 4. Small-signal model of the proposed three-stage class AB amplifier.](image)

Unlike the pseudo-class AB amplifier in Fig. 1, the intermediate non-dominant poles of the proposed class AB amplifier depend on the compensation capacitors and resistors, but not on $C_{OUT}$. Stability is limited by $\omega_{P4}$, which decreases in value as $C_{OUT}$ increases. The introduction of the third LHP zero in the proposed class AB amplifier allows the dominant pole location to be higher, resulting in a higher UGF. Fig. 5 illustrates the pole/zero locations of the pseudo-class AB and proposed class AB amplifiers.

![Fig. 5. Diagram illustrating pole/zero locations (not to scale).](image)

The expression for the phase margin of the amplifier is

$$PM \approx 90^\circ - \sum_{i=2,3,4} \tan^{-1} \left( \frac{\omega_{Pi} \omega_{Zi}}{\omega_{P2}} \right) + \sum_{i=1,2,3} \tan^{-1} \left( \frac{\omega_{P2}}{\omega_{Zi}} \right). \quad (8)$$

<table>
<thead>
<tr>
<th>Poles</th>
<th>Freq</th>
<th>Zeros</th>
<th>Freq</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\omega_{P1} = -\frac{1}{\frac{1}{R_1}C_{C1}g_{m2}R_{GD}g_{m3}R_{OUT}}$</td>
<td>1.1 kHz</td>
<td>$\omega_{Z1} = -\frac{1}{\frac{1}{R_1}C_{C1}C_{C1}+R_{GD}C_{C2}C_{C2}+R_{GD}C_{C3}C_{C3}}$</td>
<td>1.5 MHz</td>
</tr>
<tr>
<td>$\omega_{P2} = -\frac{1}{R_{C2}C_{C2}R_{GD}C_{C3}}$</td>
<td>1.6 MHz</td>
<td>$\omega_{Z2} = -\frac{1}{(R_{C1}C_{C1}R_{GD}C_{C2})+(R_{C2}C_{C3}R_{GD}C_{C3})+(R_{GD}C_{C3}R_{GD}C_{C3})}$</td>
<td>5.8 MHz</td>
</tr>
<tr>
<td>$\omega_{P3} = -\frac{1}{R_{GD}C_{C3}C_{C3}}$</td>
<td>6.6 MHz</td>
<td>$\omega_{Z3} = -\left( \frac{1}{R_{C1}C_{C1}} + \frac{1}{R_{C2}C_{C2}} + \frac{1}{R_{C3}C_{C3}} \right)$</td>
<td>38.5 MHz</td>
</tr>
<tr>
<td>$\omega_{P4} = -\frac{1}{R_{GD}C_{C2}R_{GD}C_{C3}}$</td>
<td>18.5 MHz</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
IV. RESULTS

The amplifiers of Figs. 1 and 3 were fabricated in a 0.5 μm 2P3M process with unit-size NMOS and PMOS device dimensions of 10 μm/1.2 μm and 30 μm/1.2 μm, respectively. The bias currents \( I_b, I_{b1}, I_{b2} \) and \( I_{b3} \) of the amplifier are 10 μA, 40 μA, 20 μA and 20 μA, respectively, and the output stage has a dimension ratio of \( K = 4 \). All capacitor and resistor values are given in Table III, which shows a reduction in total capacitance by 50% from 25 pF for the pseudo-class AB amplifier to 12 pF for the proposed class AB amplifier.

**TABLE III**

<table>
<thead>
<tr>
<th>Capacitance, Resistance Values of Amplifiers in Figs. 1 and 3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RC1</strong></td>
</tr>
<tr>
<td>---------</td>
</tr>
<tr>
<td>20 kΩ</td>
</tr>
<tr>
<td>1 kΩ</td>
</tr>
</tbody>
</table>

A. Simulation Results

AC analysis of the proposed class AB amplifier confirms a phase margin that is greater than 45° for a resistive load range of 500 Ω—1 MΩ and a capacitive load range of 1 pF—200 pF. Magnitude and phase plots of the proposed class AB amplifier are shown in Fig. 6 for three different loads of 25pF||1kΩ, 100pF||10kΩ and 200pF||1MΩ.

![Fig. 6. Simulated magnitude and phase plot of the proposed three-stage class AB amplifier, driving 25pF||1kΩ, 100pF||10kΩ and 200pF||1MΩ.](image)

Table IV summarizes the AC simulation results of the two amplifiers driving a load 200pF||1MΩ. The DC gain and phase margin are comparable. On the other hand, the unity-gain frequency (UGF) of the proposed class AB amplifier is 4.3 MHz, 91% higher than the pseudo-class AB amplifier. The gain margin of the class AB amplifier is 19 dB, whereas that of the pseudo-class AB amplifier is 40 dB. This difference can be attributed to the location of \( \omega_{P1} \) relative to the UGF, since \( \omega_{P2} \) and \( \omega_{P3} \) are approximately cancelled by \( \omega_{Z2} \) and \( \omega_{Z3} \). DC simulation results in Fig. 7 show the sourcing, sinking and total bias currents of the pseudo-class AB amplifier of Fig. 1 with \( K=4 \) and the proposed class AB amplifier when driving a 1 kΩ resistive load. Because of the current mirror in the last stage, the pseudo-class AB amplifier has a total bias current that is proportional to the output current. Despite the

![Fig. 7. DC simulation result of sourcing, sinking and total bias currents of (a) pseudo-class AB and (b) proposed class AB amplifiers, driving 1 kΩ.](image)

**TABLE IV**

| Simulation Results of Pseudo-Class AB and Proposed Class AB Amplifiers with ±1.25 V Driving 200pF||1MΩ Load |
|---------------------------------------------------------------|
| **DC gain** | 102 dB | 97 dB |
| **UGF** | 2.2 MHz | 4.3 MHz |
| **Phase margin** | 46° | 45° |
| **Gain margin** | 46 dB | 19 dB |

1:4 transistor ratio in the current mirror \( M_0,M_{11} \), transistor \( M_{11} \) moves into the triode region for large negative \( V_{1N} \), causing \( I_Q \) to be nearly equal to \( I_{Sink} \). On the other hand, the proposed class AB amplifier has nearly constant total bias current irrespective of the load current as shown in Fig. 7, confirming the true class AB characteristic of the proposed class AB amplifier.

![Fig. 8. Micrograph of the circuits in Figs. 1 and 3.](image)

B. Experimental Results

The micrograph of the fabricated circuits are shown in Fig. 8. The chip was tested with supply voltages of ±1.25 V and an input bias current of 10 μA. The dc sourcing, sinking and total bias currents of both amplifiers were measured and the results tabulated in Table V, for a 25pF||1kΩ load. At \( V_{OUT} = 0 \), the total bias current is 175 μA for both amplifiers. Four measurements of total bias current with \( V_{OUT} = 0 \) taken on two randomly selected chips showed a maximum variation of less than ±2%. The measured maximum output currents for both amplifiers are approximately 1.1 mA from either rails when driving a 1 kΩ load. The total bias currents of the pseudo-class AB amplifier when sourcing and sinking the maximum currents are 76 μA and 1.05 mA, respectively, whereas, those of the proposed class AB amplifier are 95 μA and 98 μA, respectively.
Transient measurements were performed on the proposed amplifier in an inverting configuration with unity gain using two 200 kΩ resistors. The amplifier was tested with a square-wave input for different combinations of capacitive and resistive loads; the output waveforms for three of the combinations are shown in Fig. 9. From Fig. 9, we see that the output is stable for a wide range of capacitive and resistive loads. The measured slew rates of the class AB amplifier for a load of 25pF/1kΩ are 2.7 V/µs and 3.3 V/µs.

![Fig. 9. Measured output waveforms (intentionally offset) of the three-stage class AB amplifier for 25pF/1kΩ, 100pF/1kΩ and 200pF/1MΩ loads.](image)

### Table V
**Summary of Simulation and Measured Results of Amplifiers in Figs. 1 and 3, Driving a Load of 25pF/1kΩ**

<table>
<thead>
<tr>
<th>Supply Voltage</th>
<th>Total C&lt;sub&gt;CUT&lt;/sub&gt;</th>
<th>R&lt;sub&gt;OUT&lt;/sub&gt;</th>
<th>C&lt;sub&gt;OUT&lt;/sub&gt;</th>
<th>Area</th>
<th>DC gain</th>
<th>UGF</th>
<th>Phase margin</th>
<th>Gain margin</th>
<th>DC CMRR</th>
<th>THD @ V&lt;sub&gt;OUT&lt;/sub&gt; = 2Vpp</th>
</tr>
</thead>
<tbody>
<tr>
<td>±1.25 V</td>
<td>25 pF</td>
<td>500 Ω–1 MΩ</td>
<td>1 pF–200 pF</td>
<td>0.05 mm&lt;sup&gt;2&lt;/sup&gt;</td>
<td>67.3 dB</td>
<td>2.6 MHz</td>
<td>99°</td>
<td>30 dB</td>
<td>71 dB</td>
<td>–45.7 dB –47.1 dB</td>
</tr>
</tbody>
</table>

### Measured Results

- I<sub>b,TOT</sub>(V<sub>OUT</sub> = 0) = 175 µA
- I<sub>b,TOT</sub>ISRC<sub>Max</sub> = 78 µA
- I<sub>SRC<sub>Max</sub> = 0.05 mA
- I<sub>SINK<sub>Max</sub> = 1.10 mA
- FOM = 1.03
- PSRR @ 1 kHz = 78.2 dB
- PSRR @ 10 kHz = 58.7 dB
- PSRR @ 100 kHz = 31.3 dB

### V. Discussion and Conclusion

The proposed class AB amplifier is similar to the pseudo-class AB amplifier in that it operates at low supply voltages, has simple biasing, a low transistor-count, wide output swing and low total bias current. Simulated and measured results of the proposed class AB amplifier are comparable with the pseudo-class AB amplifier in terms of gain, phase margin, and maximum output current as summarized in Tables IV and V.

From [19], we adopted the Figure Of Merit (FOM) to compare the current efficiency of the class AB amplifiers as the ratio of maximum load current to maximum total bias current,

\[
FOM = \frac{I_{LOAD,Max}}{I_{b,TOT,Max}}
\]

When driving a load of 25pF/1kΩ, the proposed class AB amplifier has an FOM of 6.4, whereas the pseudo-class AB amplifier has an FOM of 1.03. In addition, the CMRR and THD of the proposed amplifier are better than the pseudo-class AB amplifier, and the UGF and slew rate are almost double. Thus, the total compensation capacitance of the proposed class AB amplifier is 12 pF, 50% less than the pseudo-class AB amplifier, thereby reducing the overall footprint.

### References