Investigating the Option of Removing the Antialiasing Filter From Digital Relays

Sukumar M. Brahma, *Senior Member, IEEE*, Phillip L. De Leon, *Senior Member, IEEE*, and Rajesh G. Kavasseri, *Senior Member, IEEE*

***Abstract*—Digital relays traditionally employ sampling rates of less than 100 samples/cycle. In order to avoid aliasing due to fault transients, these relays employ an analog antialiasing filter before critical-sampling (Nyquist rate) the input waveforms coming from instrument transformers. In many applications of electrical engineering, oversampling (greater than the Nyquist rate) has long been used to simplify the requirements of an antialiasing filter with a sharp cutoff; in some cases, the filter can even be eliminated. This paper investigates this option for a digital relay. The performance of a traditional digital relay is compared with a method that uses oversampling without using an antialiasing filter. By processing a comprehensive array of fault waveforms from Electromagnetic Transients Program simulations, a suitable oversampling rate is suggested. A comparison of phasor estimates using the traditional relay and the proposed method is made for different operating and fault conditions. The results suggest that oversampling can eliminate the antialiasing filter traditionally employed in digital relays.**

***Index Terms*—Aliasing, analog-to-digital converter (ADC), digital relay, discrete Fourier transform (DFT), power system protection.**

I. Introduction

DIGITAL relays use sampling rates ranging from 8 samples/cycle to as high as 96 samples/cycle [1]. During the inception of a fault, the voltage and current waveforms are superimposed by transients. The amount and duration of transients depend on factors, such as the instant of fault with respect to the voltage waveform, the type of fault, the location of fault on the line, and the damping available in the system. Faults occurring at instants when the voltage waveform is around its peak value are the most severe in terms of transients. Typically, voltage waveforms experience more severe transients than current waveforms. Digital relays use the discrete Fourier transform (DFT) of the sampled signal to estimate the phasor value of the fundamental. To avoid aliasing, especially during a fault, all digital relays employ an analog (low-pass) antialiasing filter before sampling the voltages and currents with an analog-to-digital converter (ADC) [1], [2]. This type of filter introduces a time-delay of 1.5–2 ms in the phasor estimation depending on the sampling rate chosen [2]. This filter can also be relatively expensive.

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S. Brahma and P. De Leon are with the Klipsch School of Electrical and Computer Engineering, New Mexico State University, Las Cruces, NM 88003 USA (e-mail: sbrahma@nmsu.edu; pdeleon@nmsu.edu).

R. Kavasseri is with the Department of Electrical and Computer Engineering, North Dakota State University, Fargo, ND 58102 USA (e-mail: rajesh.kavasseri@ndsu.edu).

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In many applications, oversampling (i.e., $f_s \gg 2f_n$), where f_s and f_n are the sampling and Nyquist frequencies, respectively, has long been used to simplify the requirement of an antialiasing filter with a sharp cutoff at f_n. If the oversampling rate is selected so that any aliased frequencies are extremely small or below the noise floor, then the antialiasing filter can be made less sharp or, in some cases, even be eliminated, reducing cost and delay [3]. Many commonly available ADCs utilize oversampling for these reasons.

Very inexpensive ADC chips are currently available that use oversampling up to a few hundred kilohertz. The digital music industry today is able to produce excellent sound reproduction by using very simple or no analog prefiltering in their products. Since adopting inexpensive oversampling can eliminate a comparatively more expensive analog filter and the associated time delay, it is worthwhile to investigate the possibility of removing antialiasing filters from digital relays through oversampling. This paper investigates this possibility.

A Power System Relaying Committee (PSRC) report on software models used in relays indicates that oversampling is used in the newest generation of relays, but the main purpose of oversampling is oscillography [4]. These relays still use an analog antialiasing filter, and the sampling rate used for phasor estimation is obtained by decimating the data sampled at a higher frequency. In our extensive literature search, including a patent search, there is no published document that investigates the phasor-estimation function of a digital relay without using analog prefiltering.

This paper describes the process where a rationally chosen oversampling rate is tried out on a comprehensive array of fault waveforms generated by using the Electromagnetic Transients Program (EMTP). Through these trials, we show that phasor estimates by using the chosen oversampling rate and without using an antialiasing filter are practically the same as the phasor estimates from a conventional digital relay that uses an antialiasing filter. Factors, such as fault type, fault location, fault instant, fault resistance, and prefault conditions are varied while generating the fault waveforms. Based on the similarity of the phasor estimates for these various conditions, conclusions are drawn to emphasize the effectiveness and feasibility of the proposed approach.

II. Simulation Approach

In order to obtain a preliminary estimate of the required sampling rate to avoid aliasing, the spectral content of the sampled waveform should be measured. In order to perform such spectral analysis, a fault-voltage waveform was obtained by using EMTP simulation. A 240-kV, 225-km, two-terminal transmission line with substantially different source impedances at both ends was simulated on PSCAD/EMTDC by using the long transmission-line model. PSCAD/EMTDC is a time-tested graphical user interface for EMTP with additional components. The parameters of the test system are given in the Appendix. The load condition was created by a phase-angle difference of 15° between the two ends. A line-to-ground fault on phase A was simulated 50 km from one end, when the A-phase voltage was around its peak. This fault instant ensures severe transients in the voltage waveform. The A-phase voltage waveform was sampled at an extremely high rate of 96 kHz (1600 samples/cycle) using an appropriate timestep in the simulation. This waveform and its spectral analysis for the first cycle after the fault are shown in Fig. 1(a) and (b), respectively. The fault instant is 0.1024 s in the simulation. The window size spans one cycle, which, in this case, corresponds to 1600 samples. For simplicity, we use a rectangular window and do not average the DFT. The DFT is described by

$$V_h = \frac{2}{N}\sum_{n=0}^{N-1} v(n)e^{-jh2n\pi/N}. \quad (1)$$

In (1), V_h is the phasor estimate of the hth harmonic, $N = 1600$, and $v(n)$ is the value of the nth data sample. Fig. 1(b) shows the normalized voltage magnitude in decibels on the y axis and the frequency (log-scale) on the x axis. This means, as can be seen in Fig. 1(b), the fundamental component (60 Hz) of the voltage waveform has 0-dB magnitude. This form of display provides a better comparison of the energy in the harmonics and the energy in the fundamental.

The Nyquist rate for the selected sampling rate of 96 kHz is 48 kHz. Fig. 1(b) shows the spectral energy up to 48 kHz. If we assume an 8-bit ADC, the signal-to-quantization noise ratio can be approximated as $8\times 6 = 48$ dB [3]. If the signal of interest spans the full-scale range, as a first-order approximation, the aliased components are insignificant based on our observation of the signal energy beyond 5 kHz. Beyond 20 kHz, the signal energy drops to a very low value. Based on this observation, an oversampling rate of around $2 \times 20 = 40$ kHz should suffice. However, since $f_s = 48$ kHz is a standard sampling rate in audio applications for which very low cost ADCs are widely available, an oversampling rate of 48 kHz was selected. With this sampling rate, the harmonics beyond 24 kHz will be aliased. Clearly, from Fig. 1(b), such harmonics are almost nonexistent.

Based on the aforementioned rationale, a variety of fault-voltage waveforms was analyzed by using the following methods:

1) As mentioned before, a traditional relay receives samples at its designed sampling rate (16 samples/cycle, or 960 Hz is considered in this paper). The analog waveform, therefore, needs to be filtered to avoid aliasing. For a sampling rate of 960 Hz, the cutoff frequency of the low-pass antialiasing filter needs to be 480 Hz or lower. Since we did not have the hardware setup to model the traditional relay this way, we employed an alternate method: Digital waveforms were created by using an extremely high sampling rate of 96 kHz (1600 samples/cycle) by selecting an appropriate timestep in the simulation. This would ensure practically zero aliasing as indicated in Fig. 1(b). These waveform samples were digitally filtered by using a second-order Butterworth low-pass filter with a cutoff frequency of 240 Hz, downsampled to 16 samples/cycle, and processed with DFT to estimate the phasor value of the fundamental. This process will effectively model the traditional relay that uses an analog second-order Butterworth antialiasing filter with a cutoff frequency of 240 Hz, and uses $f_s = 960$ Hz. A cutoff frequency of lower than $f_s/2 = 480$ Hz was chosen because the second-order filter does not have a very sharp cutoff.
2) Waveform was oversampled at $f_s = 48$ kHz and directly processed with the DFT—no antialiasing filter was assumed. This models the proposed approach.

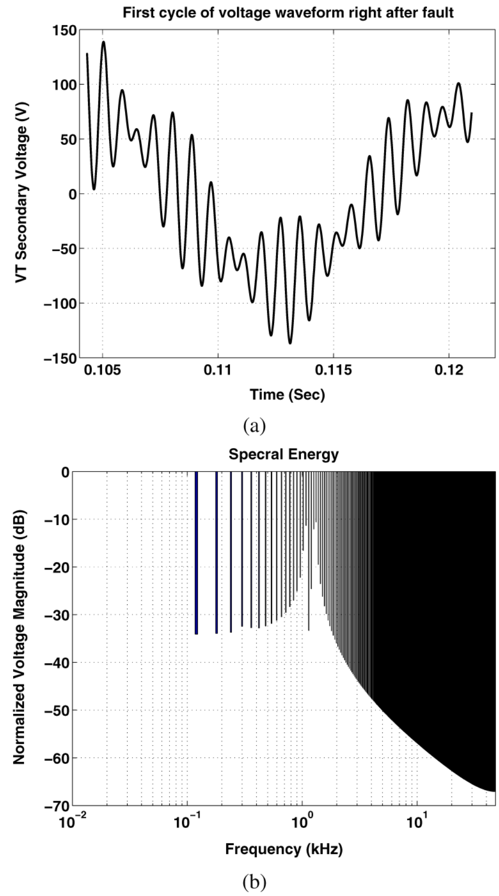
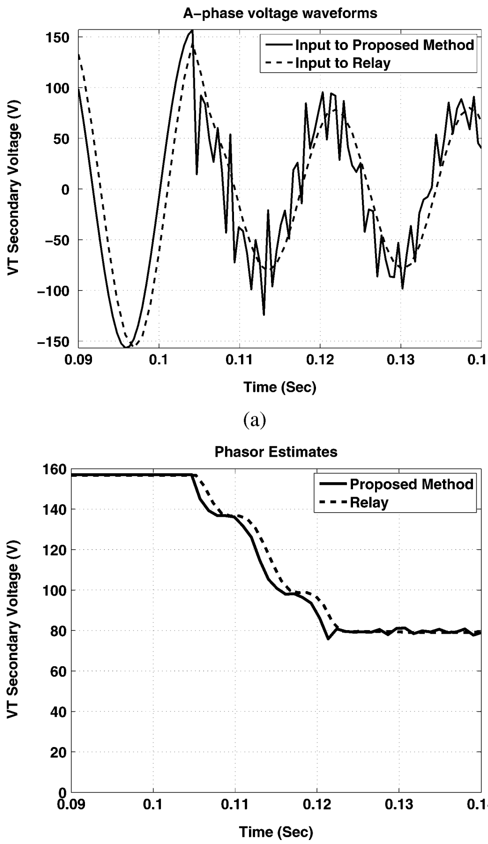


Fig. 1. Voltage waveform and its spectral energy using a sampling rate of 96 kHz.

The DFT algorithm was coded by using MATLAB. The phasor estimates using the above two approaches were compared for a very comprehensive array of fault waveforms.

III. Simulation Results

First, to illustrate the effect of aliasing on the phasor estimates, we selected $2\times$ oversampling, that is, $f_s = 960\,\text{Hz}\times 2 = 1.92$ kHz. Fig. 1(b) shows substantial signal energy above 1.92/2 = 0.96 kHz. With this sampling rate, Fig. 2(a) shows the input waveforms to the relay (filtered) and to the proposed method (unfiltered), and Fig. 2(b) shows the phasor estimates; both referred to the secondary of the voltage transformer (VT). There is obvious discrepancy in the phasor estimates. Fig. 3 shows the results for $f_s = 48$ kHz, that is, $50\times$ oversampling. The phasor estimates of both signals in Fig. 3(a), shown in Fig. 3(b), are practically the same, except for the one-cycle transition period



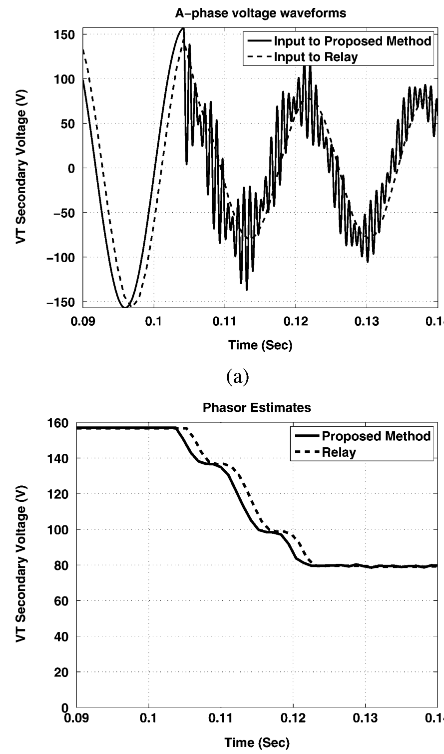
(a)

(b)

Fig. 2. Phasor estimation with a traditional relay and with the proposed approach for a sampling rate of 1.92 kHz.

from the prefault to fault condition. It can also be observed that the phasor estimation by using the proposed approach is faster, since it avoids the delay associated with the antialiasing filter.

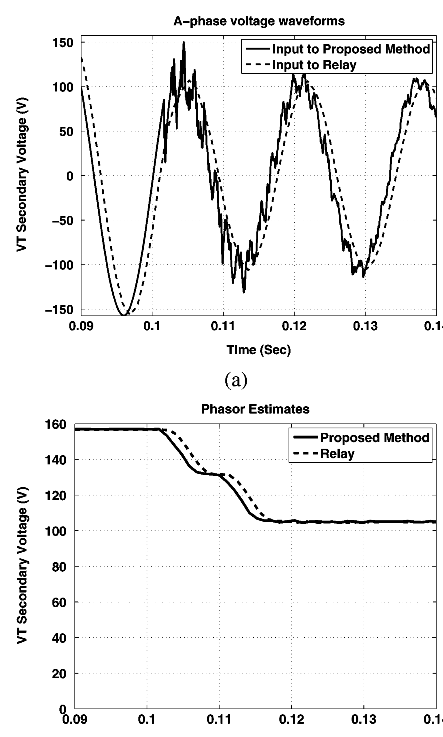
The transient content in a fault waveform can vary with the fault location, fault instant, fault type, prefault conditions, and fault resistance. Therefore, it is important to test the chosen sampling rate with respect to these various conditions. Therefore, the sampling rate of 48 kHz was applied to voltage waveforms corresponding to such conditions, and was found to provide practically the same phasor estimates as from the traditional relay. Each type of fault (LLL, LL, LG, LLG) was created at 5%, 50%, and 95% distance from the sending end of the simulated transmission line. Each fault was created at a near zero crossing of the voltage waveform, around the peak of the waveform, and at an instant half way between. Fault resistances up to 50 Ω were considered for faults involving ground, and up to 10 Ω for other types. These values are higher than the typical fault resistance values quoted in [5]. Fig. 4 shows the results for an LG fault at 100 km from the sending end. Fig. 5 shows the results for an LLL fault at 150 km from the sending end. Both of these faults take place at a point between the zero crossing and the peak of the voltage waveform. The LLL fault was created with a prefault-angle difference between two ends of the transmission line being 18°. It can be seen that $f_s = 48$ kHz gives satisfactory results in both cases. This was true for all of the cases tested.



(a)

(b)

Fig. 3. Phasor estimation with a traditional relay and with the proposed approach for a sampling rate of 48 kHz.



(a)

(b)

Fig. 4. Phasor estimation with a traditional relay and with the proposed approach for LGF at 100 km from the sending end.

It should be mentioned here that some lower sampling rates also gave good results. We tried the three most commonly found

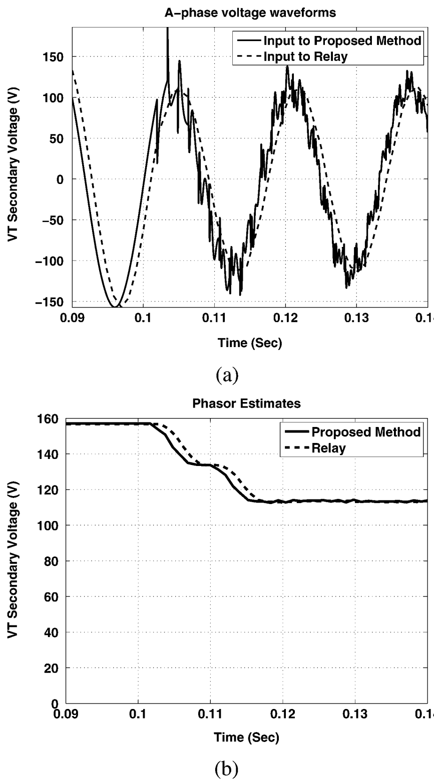


Fig. 5. Phasor estimation with a traditional relay and with the proposed approach for LLLF at 150 km from the sending end.

audio-band sampling rates: 48 kHz, 24 kHz, and 18 kHz. There was practically no difference in the results obtained with 24 kHz and 48 kHz for the cases we investigated. There was, however, a perceptible difference with a sampling rate of 18 kHz. The decision was made to select $f_s = 48$ kHz to include a safety margin.

It is also important to mention here that the proposed method does not require performing the DFT after every new sample enters the data window. At the proposed rate, that would mean 800 phasor estimates per cycle, which is not necessary. The results presented here were obtained by performing DFT only 16 times per cycle, just like a traditional relay. However, the data window with the proposed method has 800 samples compared to 16 samples in the traditional relay. The DFT process is shown as

$$V = \frac{2}{N}\sum_{n=0}^{N-1} v(n)e^{-j2n\pi/N}. \quad (2)$$

In (2), V is the phasor estimate of the fundamental, N is the number of samples in the data window, and $v(n)$ is the value of the nth data sample. We use (2) with a sliding data window. With a sampling rate of 16 samples per cycle, the DFT will be performed after every new sample enters the data window. In our case, we wait for $800/16 = 50$ new samples to enter the data window before we perform DFT. With 16 samples/cycle, N in (2) is equal to 16; in our case, it is equal to 800.

For the CPU, the extra calculation burden comes from the increased window size (800 v/s 16 samples). In (2), the terms inside the summation symbol constitute one real term $(v(n))$, and the other complex term (exponential). This means there are two Multiply and one Add operations to implement the term inside the summation symbol once. For the larger window, $(N = 800)$, the total multiply-accumulate (MAC) operations required are $800 \times 2 = 1600$ instead of $16 \times 2 = 32$ for the smaller window $(N = 16)$. The added calculation burden is therefore $1600 - 32 = 1568$ MAC operations. If we assume the CPU/DSP effectively executes one MAC instruction per clock cycle, a 100-MHz processor (as an example), increases the computation time to $(1600 - 32)/(100 \times 10^6) = 15.68$ μs for the calculation of (2). Since we calculate the phasor value only 16 times per cycle with the proposed method, the time interval between successive calculations of (2) is 1/60/16 $= 1042$ μs for a 60-Hz system. Thus, the additional calculation time will not affect the real-time implementation at all. With current digital hardware technologies that use a much higher processor speed, this is even more of a nonissue.

The increase in the VA burden of the relay due to the increased window size is unlikely to be significant. It is likely that the existing CPU/DSP in the digital relay can accommodate the increased computation due to the increased window size, since it is relatively small. In this case, there would be no additional power consumption. Otherwise, newer CPU/DSP chips, which can accommodate the increased computation, typically consume less than 1 W. The major part of the VA burden is due to the operational amplifiers used in ADCs rather than the chip.

The cost of commercially available ADC chips employing the chosen sampling rate is typically less compared to the cost of an analog antialiasing filter. Numerical relays require multiple antialiasing filters, depending on the number of input channels used. Removal of these filters, therefore, will result in a savings in cost as well as savings in boardspace.

IV. Conclusion

This paper investigates the possibility of removing the analog antialiasing filter from the traditional digital relay without sacrificing the quality of the phasor estimation performed by the relay. Oversampling of the analog waveform is used to achieve the objective. Using extensive testing on fault waveforms generated by using PSCAD/EMTDC, a suitable oversampling rate is suggested. It is shown that the performance of the traditional relay with the antialiasing filter and the performance using the proposed approach are equivalent. This indicates that the approach is technically sound. The potential advantage of this approach is savings in cost and space. Oversampling also provides greater design flexibility for low-cost digital filters that can provide better performance than traditional relays. Our future efforts will be aimed at designing these digital filters.

Appendix

Transmission line—225 km:
positive-sequence impedance: 0.0358 + j0.4918 Ω/km;
zero-sequence impedance: 0.352 + j1.3456 Ω/km;
positive-sequence capacitive susceptance: 6.841 μS/km;
zero-sequence capacitive susceptance: 4.24 μS/km.
Sending end source:
positive-sequence impedance: 5 + j27.7095 Ω;
zero-sequence impedance: 10.5 + j56.55 Ω.
Receiving end source:
positive-sequence impedance: 0.6 + j9.3119 Ω;
zero-sequence impedance: 1.3 + j18.85 Ω.

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Sukumar M. Brahma (S'00–M'04–SM'07) received the B.Eng. degree in electrical engineering from Lalbhai Dalpatbhai College of Engineering, Ahmedabad, India, in 1989, the M.Tech. degree in electrical engineering from the Indian Institute of Technology, Bombay, in 1997, and the Ph.D. degree in electrical engineering from Clemson University, Clemson, SC, in 2003.

From 1990 to 1999, he was a Lecturer in the Electrical Engineering Department at Birla Vishvakarma Mahavidyalaya Engineering College, Vallabh Vidyanagar, India. From 2003 to 2007, he was Assistant Professor at Widener University, Chester, PA. Currently, he is Assistant Professor at New Mexico State University, Las Cruces.

Dr. Brahma is a member of Sigma Xi, Chair of the IEEE Power Engineering Society's Life Long Learning Subcommittee, Vice Chair of the Distribution System Analysis Subcommittee, and is with several working groups of the Power System Relaying Committee.

Phillip L. De Leon (SM'03) received the B.S. degree in electrical engineering and the B.A. degree in mathematics from the University of Texas at Austin, in 1989 and 1990, respectively, and the M.S. and Ph.D. degrees in electrical engineering from the University of Colorado at Boulder, in 1992 and 1995, respectively.

Previously, he was witjh AT&T (later Lucent Technologies) Bell Laboratories, Murray Hill, NJ. Currently, he is a Professor in the Klipsch School and Director of the Advanced Speech and Audio Processing Laboratory at New Mexico State University, Las Cruces. His research interests are in speech processing and embedded systems.

Dr. De Leon is a member of Eta Kappa Nu.

Rajesh G. Kavasseri (M'02–SM'07) received the B.E. degree in electrical engineering from Visvesvaraya Regional College of Engineering, Nagpur, India, in 1995, the M.Sc. degree in electrical engineering from the Indian Institute of Science, Bangalore, India, in 1998, and the Ph.D. degree in electrical engineering from Washington State University, Pullman, in 2002.

He has been with the Department of Electrical and Computer Engineering at North Dakota State University, Fargo, since 2002, where he is an Associate Professor. His primary research interests focus on the dynamics, stability, and control of electric power systems.

Dr. Kavasseri is the Vice-Chair of the IEEE Red River Valley Section.